MF617
3-Phase Brushless DC Motor Controller
Data Sheet

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Revision History:

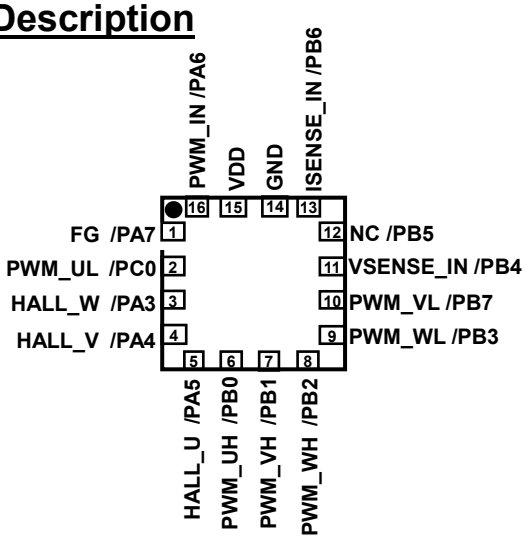
Revision	Date	Description
0.00	2022/06/29	Preliminary version
0.01	2022/08/10	1. Add Section 6.1. Marking Information 2. Amend Chapter 7 3. Other known details bug correct.

1. Key Features

- 3-Phase brushless DC motor with hall IC interface
- PWM or voltage control input
- FG/RD/ALM/RALN/RXX/RRXX output
- Alarm output
- Reverse brake control
- Software hall angle forward and backward
- Close loop or/and open loop control
- Current limit and over-current protection
- Under voltage lock out protection
- Over voltage lock out protection
- Soft-start, lock-protect and auto-restart
- System protection
  - Low-voltage detection with reset
  - Illegal opcode detection with reset
- MTP Programming
  - Support 6-wire factory programming mode
  - Support 4-wire in-system programming mode
- DC Fan Applications
  - Operating voltage range: 3.5V~6V
  - Operating temperature range: -40°C~105°C
- Ordering/ Package Information
  - MF617-2J16A: QFN4*4 (16P-0.65pitch)

MF617 is a 3-phase BLDC motor controller based on 8-bit 8-FPPA MCU which can be programmed by 6-wire factory mode or 4-wire ISP mode. MF617 receives motor position signal from Hall IC and can control the six step square wave flexibly to make the best efficiency of the motor. Through the PADAUK patented AP development system, it can easily set any speed curve, output signal and protection parameters etc., and it can observe the motor response online immediately. Using the MF617's development system, it's much easier and adjustable for application.

2. Pin Diagram and Pin Description



MF617-2J16A: QFN4*4 (16P-0.65pitch)

Pin Name	I/O	Description
FG / PA7	Output	Rotation speed detection
PWM_UL / PC0	Output	U output signal to control the low side of motor driver
HALL_W / PA3	Input	Digital input to sense motor position W
HALL_V / PA4	Input	Digital input to sense motor position V
HALL_U / PA5	Input	Digital input to sense motor position U
PWM_UH / PB0	Output	U output signal to control the high side of motor driver
PWM_VH / PB1	Output	V output signal to control the high side of motor driver
PWM_WH / PB2	Output	W output signal to control the high side of motor driver
PWM_WL / PB3	Output	W output signal to control the low side of motor driver
PWM_VL / PB7	Output	V output signal to control the low side of motor driver
VSENSE_IN / PB4	Input	Analog input to sense motor voltage
NC / PB5	I/O	Digital input/output to motor application
ISENSE_IN / PB6	Input	Analog input to sense motor current
GND	-	Ground
VDD	-	Positive power
PWM_IN / PA6	Input	PWM control input

3. Device Characteristics

3.1. Absolute Maximum Ratings

Name	Min	Typ.	Max	Unit	Notes
Supply Voltage (VDD)	3.5		6	V	**Exceed the maximum rating may cause permanent damage!!**
Input Voltage	-0.3		V_{DD} + 0.2	V	
Operating Temperature	-40		105	°C	
Storage Temperature	-50		125	°C	
Junction Temperature		150		°C	

3.2. DC/AC Characteristics

Symbol	Description	Min	Typ	Max	Unit	Conditions (Ta=25℃)
V_{DD}	Operating Voltage	3.5#	5.0	6	V	#Subject to V_{BRD} tolerance
V_{PDRV}	V_{DD} power down release voltage			0.1	V	
T_{POR}	V_{DD} power on time (V_{DD} from 0V to 5V)			500	ms	
T_{drop}	V_{DD} power on time during V_{PDRV} range	1			ms	
T_{LVR}	V_{DD} power on time during V_{LVR} range	1			ms	
f_{SYS}	System clock IHRC Internal low RC oscillator	0	 54.9K	8M	 Hz	 V_{DD} = 3.5V V_{DD} = 5.0V
P_{cycle}	Program cycle	1000			cycles	
I_{OP}	Operating Current		1.0 2.1 110 85		mA mA uA uA	f_{SYS}=1MIPS@5.0V f_{SYS}=8MIPS@5.0V f_{SYS}=ILRC ~ 55KHz@5.0V f_{SYS}=ILRC ~ 54KHz@3.3V
I_{PD}	Power Down Current (by ***stopsys*** command)		1 0.61		uA uA	V_{DD}=5.0V V_{DD}=3.3V
I_{PS}	Power Save Current (by ***stopexe*** command)		18		uA	V_{DD}=5.0V; Bandgap, LVR, IHRC, ILRC, Timer16 modules are ON.
V_{IL}	Input low voltage for IO lines	0		0.2V_{DD}	V	
V_{IH}	Input high voltage for IO lines	0.8 V_{DD}		V_{DD}	V	
I_{OL}	IO lines sink current	11	14 7	17	mA	V_{DD}=5.0V, V_{OL}=0.5V, Normal V_{DD}=5.0V, V_{OL}=0.5V, Low
I_{OH}	IO lines drive current	-8	-10 -6	-12	mA	V_{DD}=5.0V, V_{OH}=4.5V, Normal V_{DD}=5.0V, V_{OH}=4.5V, Low
R_{PH}	Pull-high Resistance		32 33		KΩ	V_{DD}=5.0V V_{DD}=3.3V

Symbol	Description	Min	Typ	Max	Unit	Conditions (Ta=25℃)
V_{BRD}	Low Voltage Detect Voltage * (Brown-out voltage)	4.2 3.7 3.35 3.25 3.05 2.9	4.5 4 3.75 3.5 3.3 3.15	4.8 4.3 4.05 3.75 3.55 3.4	V	
V_{BG}	Bandgap Reference Voltage (before calibration)	1.12	1.20	1.28	V	V_{DD}=5V, 25°C
	Bandgap Reference Voltage * (after calibration)	1.17*	1.20*	1.23*		V_{DD}=3.15V ~ 5.5V, -40°C <Ta<105°C*
f_{IHRC}	Frequency of IHRC after calibration *	15.52*	16*	16.48*	MHz	25°C, V_{DD}=3.15V~5.5V
		14*	16*	17.28*		V_{DD}=3.15V~5.5V, -40°C <Ta<105°C*
f_{ILRC}	Frequency of ILRC *	31.5*	33.8*	35*	KHz	V_{DD}=5.0V, Ta=25°C
		29*	33.8*	38.4*		V_{DD}=5.0V, -40°C <Ta<105°C*
		32*	34*	35.5*		V_{DD}=3.3V, Ta=25°C
		29*	34*	40*		V_{DD}=3.3V, -40°C <Ta<105°C*
V_{ADC}	Workable ADC operating Voltage	3.15		5.0	V	
V_{AD}	AD Input Voltage	0		V_{DD}	V	
ADrs	ADC resolution			11	bit	
ADclk	ADC clock period		2		us	3.15V ~ 5.5V
t_{ADCONV}	ADC conversion time (T_{ADCLK} is the period of the selected AD conversion clock)		14		T_{ADCLK}	
AD DNL	ADC Differential NonLinearity		±3*		LSB	
AD INL	ADC Integral NonLinearity		±3*		LSB	
ADos	ADC offset*		3		LSB	-40°C <Ta<105°C*
t_{INT}	Interrupt pulse width	30			ns	V_{DD} = 5.0V
V_{DR}	RAM data retention voltage*	1.5			V	In power-down mode.
t_{WDT}	Watchdog timeout period (T_{ILRC} is the clock period of ILRC)		4096			misc[1:0]=01
			16384			misc[1:0]=10
t_{SBP}	System boot-up period from power-on		2500		T_{ILRC}	Where T_{ILRC} is the clock period of ILRC

Symbol	Description	Min	Typ	Max	Unit	Conditions (Ta=25℃)
t_{WUP}	System wake-up period					
	Normal wake-up from STOPEXE or STOPSYS suspend		2500		T_{ILRC}	Where T_{ILRC} is the clock period of ILRC
HCPos	Comparator offset*	-	±10	±20	mV	
HCPcm	Comparator input common mode*	0		V_{DD}-1.5	V	
HCPspt	Comparator response time**		100	500	ns	Both Rising and Falling
HCPmc	Stable time to change comparator mode		2.5	7.5	us	

*These parameters are for design reference, not tested for every chip.

** Response time is measured with comparator input at (V_{DD}-1.5)/2 -100mV, and (V_{DD}-1.5)/2+100mV

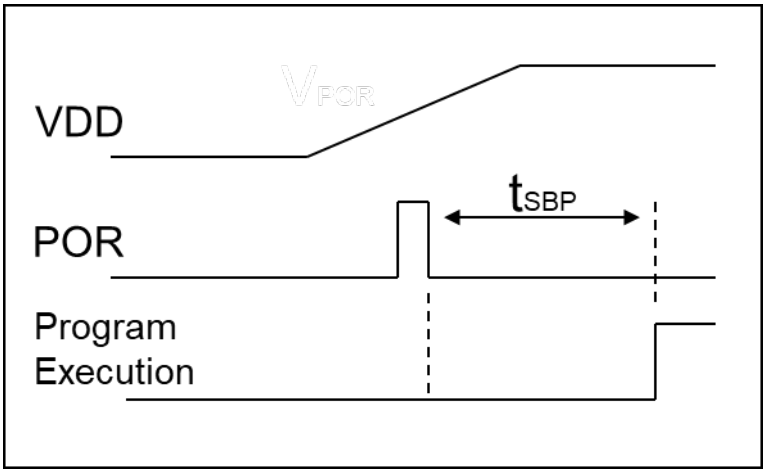
The characteristic diagrams are the actual measured values. Considering the influence of production drift and other factors, the data in the table are within the safety range of the actual measured values.

4. Reset

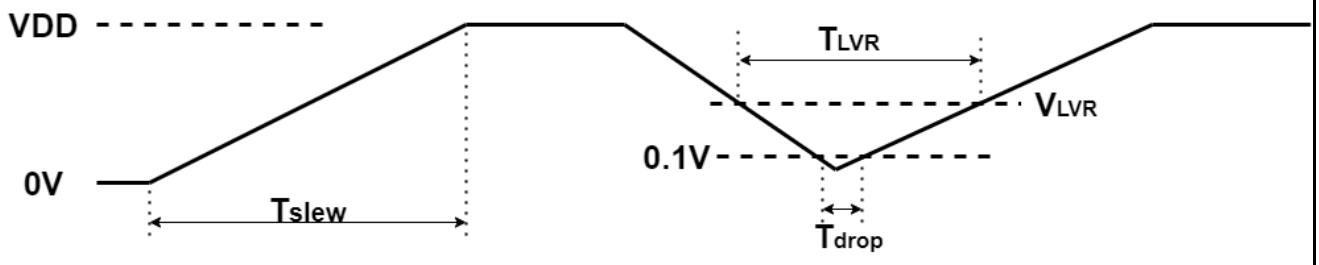
There are many causes to reset the MF617, the main two factors are: power-on reset, and LVR reset. After the reset, the system will restart.

4.1. Power On Reset - POR

POR (Power-On-Reset) is used to reset MF617 when power up, however, the supply voltage may be not stable. To ensure the stability of supply voltage after power up, it will wait TSBP time before first instruction being executed, and shown as below Figure. After boot up procedure.



Power On Reset constraint



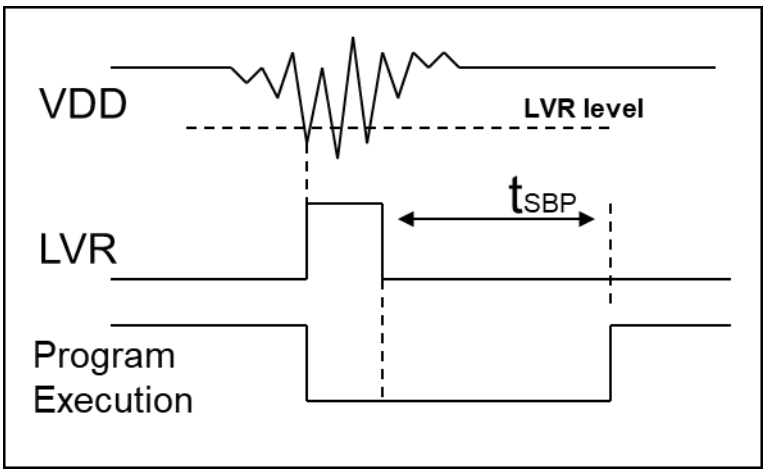
1. Tslew <= 500ms
2. VDD drop below 0.1V for T_{drop} to trigger POR again.
3. T_{drop} >=1ms

LVR constraint

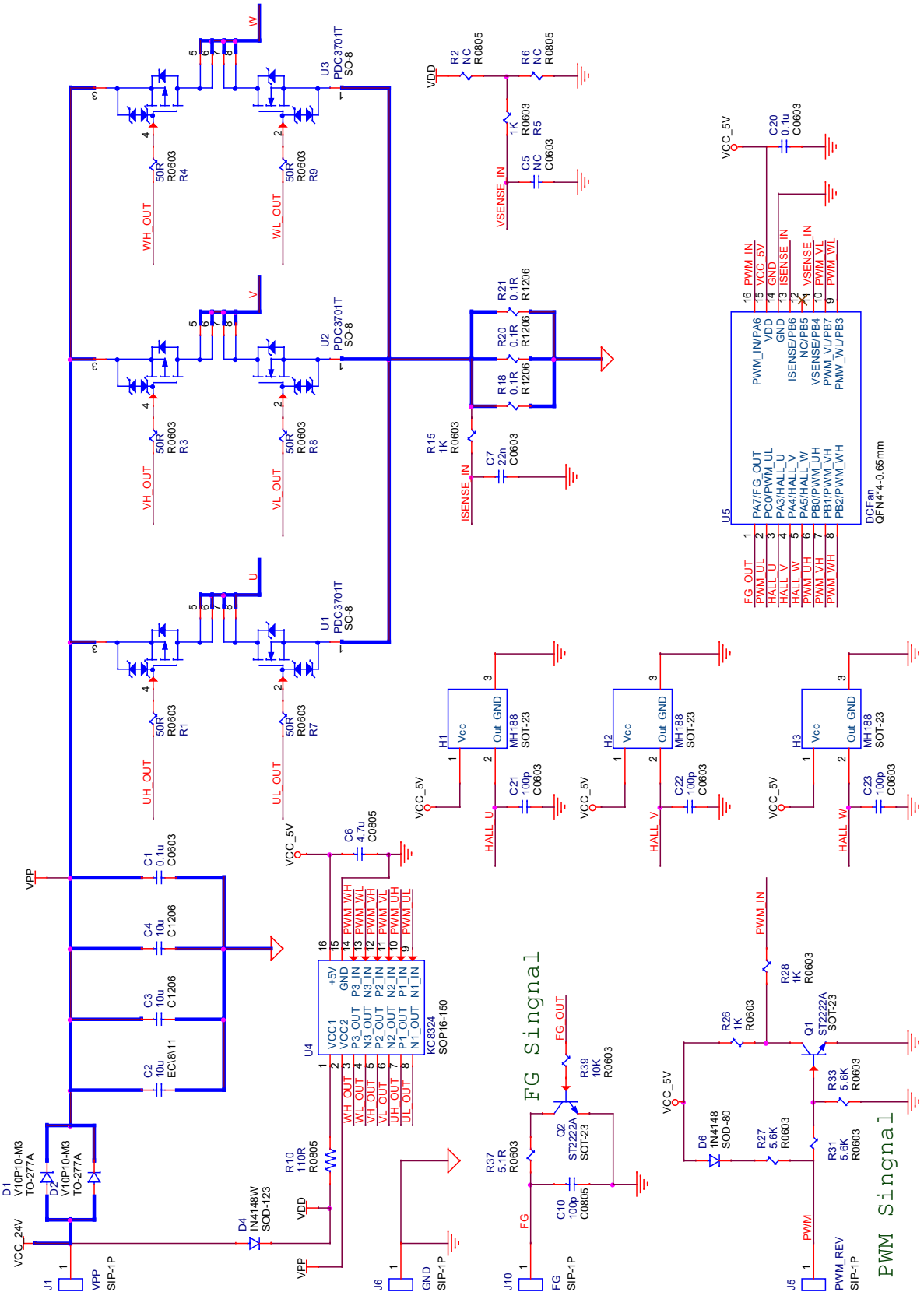
1. VDD drop below V_{LVR} for T_{LVR} to trigger LVR.
2. T_{LVR} >=1ms

4.2. Low Voltage Reset - LVR

If VDD drops below the LVR level, then the LVR Reset will occur in the system, and its timing diagram is shown as below Figure.



5. Reference Application Circuit



6. Package Marking Information

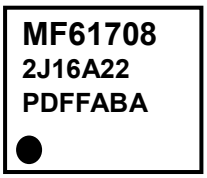
6.1. Marking Information

Effective Date: 2022/8/1

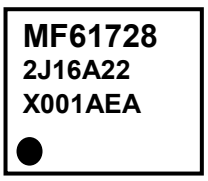
◎ Note: This specification is ONLY for MF617-2J16A.

QFN 4*4mm

Example: blank

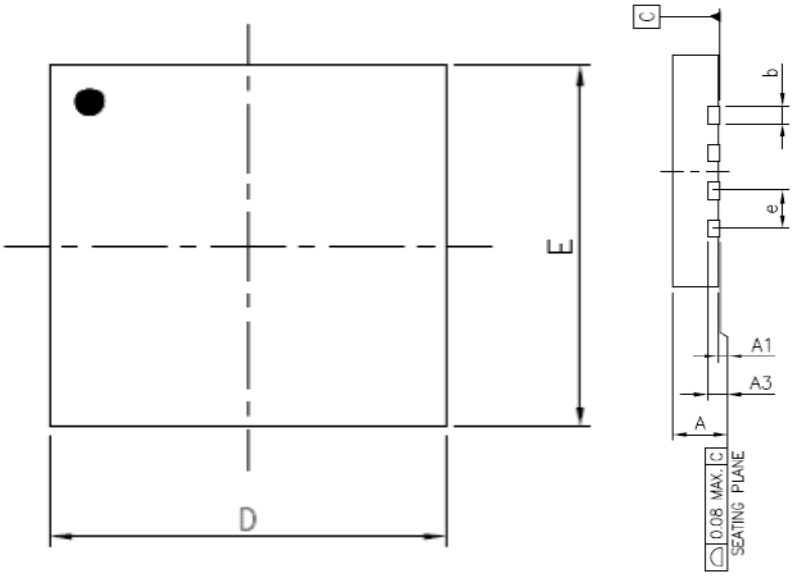


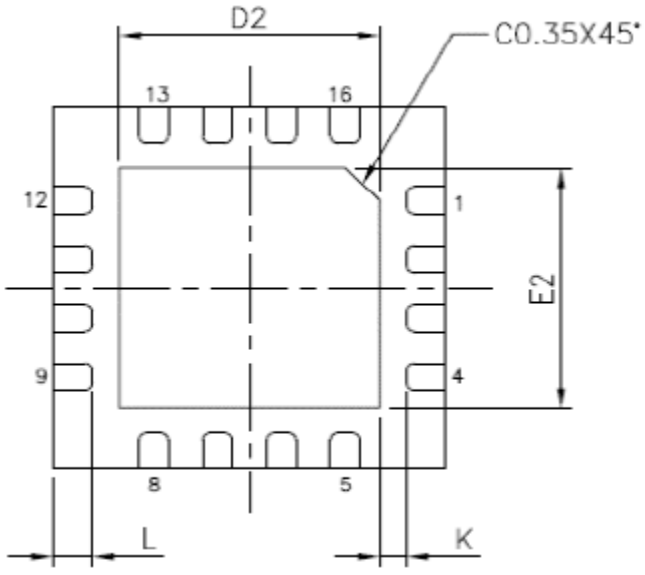
Example: code



Standard Legend	
PPPPP	MF617
CCCC	Customer's production code number (If blank that CCCC will be PDFF.)
QQ	Package type (QFN 4*4mm → 2J)
LL	Pin Count
B	Bonding information (Ex:MF617-2J16A → PADAUK Type A QFN4*4-16 package.)
yy	Year code (last 2 digits of calendar year)
ww	Week code
V	Vender code
X	Product code
A	Wafer information

6.2. QFN4*4 (16P-0.65pitch)





	MILLIMETERS		
SYMBOLS	MIN	TYP	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.203 REF	
b	0.25	0.30	0.35
D		4.00 BSC	
E		4.00 BSC	
e		0.65 BSC	
K	0.20	-	-
D2	2.60	2.65	2.70
E2	2.60	2.65	2.70
L	0.35	0.40	0.45

7. PCB layout guideline

7.1. PCB designer comply with IPC-7525 and IPC-7351 and IPC-7095 requirements is recommended.

7.2. QFN/DFN /SOP E-pad package PCB layout guideline:

7.2.1. Because of the rich solder paste volume under QFN/DFN/SOP thermo pad area which will raise the QFN/DFN package during reflow process, this kind of effect will cause QFN/DFN terminal floating and solderbility fail issue. To prevent the QFN/DFN floating and become solderability open short issue during SMT process, the solder past coverage between 15% to 30 % of thermo pad area is recommended. The blue color areas of Figure QFN/DFN is a just sample for stencil design. Anyway, stencil design should be fine tune by SMT house if the poor contact issue happened.

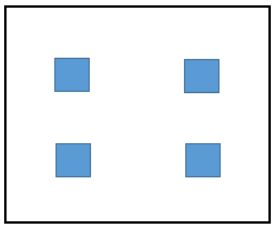


Figure QFN/DFN

7.3. PCB process

7.3.1. Stencil Design Guidelines: Refer to IPC-7525 Stencil Design Guidelines process.

7.3.2. Reflow Oven: Forced convection reflow with nitrogen is recommended for Pb-free and Green package.

7.3.3. Reflow profile: Using more than 8 zone oven is recommended for Pb-free and Green package.

7.3.4. To use IPC-A-610 is recommended for soldered electrical and electronic assemblies.

7.4. Rework and Repair Guide

7.4.1. Reballing BGA/CSP is not recommended for production applications if there are no special reball fixtures and tools. There are many rework system on market, however, special reball fixtures and tools have been designed to simplify and help control this process. For additional information, refer to IPC -7711/21A Rework and Repair Guide or IPC-7095A (Design & Assembly Process Implementation for BGA's) or search IPC website.

7.4.2. QFN/DFN Rework and Repair Guide: The Rework and Repair Guide of QFN/DFN package is the same with BGA products which need special re-work fixtures and tools, and use IR-reflow process.